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(21)Application number : 07-221048 (71)Applicant : NIKON CORP

(22)Date of filing : 07.08.1995 (72)Inventor : YONEYAMA JUICHI

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(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent an excess rush current caused when all picture elements of the solid-state image pickup device are reset.

SOLUTION: The solid-state image pickup device having plural pixels for photoelectric conversion and scanning circuits 5, 9 selecting sequentially the plural picture elements 1 is provided with a shift register as a scanning circuit to set outputs of plural circuit stages to a prescribed logic state nearly simultaneously and with a light receiving element PD as a picture element 1 and an amplifier element QA amplifying a signal charge stored in the light receiving element PD. Outputs of plural circuit stages of the shift register of the scanning circuit 5 are set to the prescribed logic state to select plural picture elements 1 and the charge of the light receiving element PD is reset while the plural selected picture elements 1 cut off the amplifier element QA.

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CLAIMS

[Claim(s)]

[Claim 1] In the solid state camera possessing the scanning circuit for making sequential selection and reading two or more pixels which perform photo electric conversion, and said two or more pixels said scanning circuit Tandem connection of two or more circuit stages is carried out, they are constituted, and coincidence is mostly equipped with the shift register which can be set as a predetermined logic state for the output of two or more of said circuit stages according to the input of a predetermined control signal. The photo detector in which said pixel accumulates the signal charge according to a lightwave signal at least respectively, While choosing two or more pixels by having the amplifier which amplifies the signal charge accumulated in this photo detector, and setting the output of two or more circuit stages of the shift register of said scanning circuit as said predetermined logic state The solid state camera characterized by reducing the rushes current at the time of reset by resetting the charge of said photo detector where said amplifier is cut off in two or more selected pixels.

[Claim 2] It is the solid state camera according to claim 1 characterized by

providing the transfer component which transmits the signal charge further accumulated in said photo detector in each of said pixel to the control electrode of said amplifier, and the reset component which resets the charge of the control electrode of said amplifier, and resetting the charge of a photo detector by setting both said transfer component and said reset component to ON.

[Claim 3] Furthermore, the solid state camera according to claim 2 characterized by including the bias voltage impression means for impressing bias voltage to said amplifier and holding said amplifier in the cut-off condition in case the charge of a photo detector is reset by setting both said transfer component and a reset component to ON.

[Claim 4] Two or more pixels which consist of a magnification mold photo-electric-conversion means to be arranged in the shape of two-dimensional in a line and the direction of a train, and to accumulate and amplify the signal charge according to a lightwave signal respectively, In the current regulator circuit prepared for each [which connected in common the output terminal of each pixel arranged in the direction of a train] train Rhine of every, and the solid state camera which carries out the selection drive of said pixel and which has level and perpendicular each scanning circuit Tandem connection of two or more

circuit stages is carried out, they are constituted, and said vertical-scanning circuit equips coincidence with the shift register which can be set as a predetermined logic state for the output of two or more of said circuit stages mostly according to the input of a predetermined control signal. The photo detector which accumulates the signal charge [pixel / said] corresponding to the lightwave signal respectively, and the amplifier which amplifies the signal charge accumulated in this photo detector, The transfer component which transmits the signal charge accumulated in said photo detector to the control electrode of said amplifier, The reset component which resets the charge of the control electrode of said amplifier is provided. The control electrode of the transfer component of the pixel of each line is connected to line Rhine which corresponds in common. Line Rhine of each line is connected to the correspondence circuit stage of said vertical-scanning circuit, and the control electrode of the reset component of all pixels is connected to a reset control signal input terminal in common. And all transfer components are set to ON through said each line Rhine by setting the output of two or more circuit stages of the shift register of said vertical-scanning circuit as said predetermined logic state. And while setting the reset component of all pixels to ON and resetting the charge of a photo detector through a transfer

component and a reset component by adding said reset control signal to the reset component of all pixels The solid state camera characterized by reducing the rushes current at the time of reset by impressing the electrical potential difference which makes this amplifier a cut-off condition to the control electrode of an amplifier through the reset component which became ON on the occasion of this reset.

[Claim 5] Two or more pixels which consist of a magnification mold photo-electric-conversion means to be arranged in the shape of two-dimensional in a line and the direction of a train, and to accumulate and amplify the signal charge according to a lightwave signal respectively, In the current regulator circuit prepared for each [which connected in common the output terminal of each pixel arranged in the direction of a train] train Rhine of every, and the solid state camera which carries out the selection drive of said pixel and which has level and perpendicular each scanning circuit Tandem connection of two or more circuit stages is carried out, they are constituted, and said vertical-scanning circuit equips coincidence with the shift register which can be set as a predetermined logic state for the output of two or more of said circuit stages mostly according to the input of a predetermined control signal. The photo

detector which accumulates the signal charge [pixel / said] corresponding to the lightwave signal respectively, and the amplifier which amplifies the signal charge accumulated in this photo detector, The transfer component which transmits the signal charge accumulated in said photo detector to the control electrode of said amplifier, The reset component which resets the charge of the control electrode of said amplifier is provided. The control electrode of the transfer component of the pixel of each line is connected to line Rhine which corresponds in common. Line Rhine of each line is connected to the correspondence circuit stage of said vertical-scanning circuit, and the control electrode of the reset component of all pixels is connected to a reset control signal input terminal in common. Each train Rhine It has a means to impress bias voltage to an amplifier through each train Rhine in order to change into a cut-off condition the amplifier of the pixel connected to each train Rhine. And all transfer components are set to ON through said each line Rhine by setting the output of two or more circuit stages of the shift register of said vertical-scanning circuit as said predetermined logic state. And while setting the reset component of all pixels to ON and resetting the charge of a photo detector through a transfer component and a reset component by adding said reset control signal to the reset component of all pixels The solid

state camera characterized by reducing the rushes current at the time of reset by making the amplifier of all pixels into a cut-off condition with said bias voltage impression means in the case of this reset.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Concerning a solid state camera, this invention is used for an electronic "still" camera etc., and instant-reset of all pixels is possible for it, and it relates to the solid state camera which can moreover reduce the rushes current at the time of reset sharply.

[0002]

[Description of the Prior Art] Drawing 6 shows the configuration of the outline of the conventional solid state camera, and shows the example of two-dimensional image sensors. The equipment of this drawing is considered as the pixel configuration of three line x3 train for simplification of explanation. Moreover, although the subscript is given to the reference mark of each component in the drawing, a subscript may be omitted when expressing on behalf of the component of the same class for simplification of explanation.

[0003] With the equipment of drawing 6 , the static induction transistor (SIT) is used as an example of a magnification mold photo detector as each pixel. That is, the static inductions transistor QS11, QS12, QS13, QS21, QS22, QS23, QS31, QS32, and QS33 which constitute each pixel are arranged in the shape of

[of three line x3 train] a matrix.

[0004] Moreover, the vertical-scanning circuit VSR for making sequential selection of the pixel of each train for every line is formed. That is, the gate of the static induction transistor arranged among the pixels arranged in the shape of a matrix at each line writing direction is connected to each circuit stage of the shift register of the vertical-scanning circuit VSR through each line Rhine GV1, GV2, and GV3 in common. For example, the gate of static inductions transistor QS11, QS12, and QS13 is connected to the vertical-scanning circuit VSR through both line Rhine GV1, and the gate of each static inductions transistor QS21, QS22, and QS23 is connected to the vertical-scanning circuit VSR through line Rhine GV2. All circuit stages are reset or preset by impression of initialization signal phiINTV, and the vertical-scanning circuit VSR can change all line Rhine GV1, GV2, and GV3 into the selection condition by it.

[0005] Moreover, the source of the static induction transistor of the pixel of each train is connected common to train Rhine LV1, LV2, and LV3 of the train, and each train Rhine is connected to the predetermined power source VEE through the constant current source CSV. Each constant current source CSV serves as a load of the static induction transistor QS of each pixel at the time of signal

read-out from each pixel. The drain of the static induction transistor QS of each pixel is connected to the predetermined power source VDD in common. The end of each train Rhine LV1, LV2, and LV3 is grounded through the transistors QRSTV1, QRSTV2, and QRSTV3 for perpendicular reset for resetting each train Rhine. Reset-signal phiRSTV for perpendicular read-out lines explained later is supplied to each transistor for perpendicular reset.

[0006] The other end of each train Rhine LV1, LV2, and LV3 is connected to the drain of each transistor QH1, QH2, and QH3 for water Hiraide force through each switch QT1, QT2, and QT3 for a transfer. The source of each transistor for water Hiraide force is connected to the common water Hiraide line of force HOUT, and this water Hiraide line of force HOUT is connected to the video outlet terminal for supplying an image pick-up signal outside. Moreover, the source of each transistors QT1, QT2, and QT3 for a transfer is grounded through each capacity CT1, CT2, and CT3.

[0007] The gate of the transistors QT1, QT2, and QT3 for a transfer of each train is connected in common, and transfer pulse phiT is supplied. Moreover, the gate of the level read-out transistors QH1-QH3 is connected to each circuit stage of the horizontal scanning circuit HSR. Like [the horizontal scanning circuit HSR]

said vertical-scanning circuit VSR, it has a shift register and, as for this shift register, the thing in which the set or reset of all circuit stages is possible is used by level initialization signal phiINTH.

[0008] When used for an electronic "still" camera, the solid state camera of drawing 6 operates by adding perpendicular start signal phiSTV to the vertical-scanning circuit VSR, and adding clock signal phiCKV for a perpendicular shift after progress of the predetermined exposure time, so that the shift register of the vertical-scanning circuit VSR may shift sequential aforementioned start signal phiSTV to each circuit stage. Sequential selection of each line Rhine GV1, GV2, and GV3 is made by this. The signal charge according to incident light is accumulated in each static induction transistor QS, and the electrical potential difference corresponding to the charge with which this static induction transistor operated as a source follower, and was accumulated is outputted to each train Rhine LV by applying a predetermined selection electrical potential difference to the gate voltage in the selected line. That is, the signal from the static induction transistor QS of the selected line is outputted to each perpendicular read-out line LV at coincidence.

[0009] And after making it flow through the transfer transistor QT of each train by

transfer signal phiT at this time and charging a signal charge at capacity CT1, CT2, and CT3, QT is intercepted, and the signal for every train is outputted to the water Hiraide line of force HOUT by setting the level read-out transistor QH to ON one by one by the vertical-scanning circuit HSR.

[0010] By the way, when such a solid state camera is used for an electronic "still" camera, after resetting all pixels at the moment of pushing a shutter, the image pick-up of a photographic subject image is performed. In the solid state camera of drawing 6 , reset of all pixels is performed as follows.

[0011] That is, the vertical-scanning circuit VSR is controlled by initialization signal phiINTV, clock signal phiCKV, and scan start signal phiSTV including a shift register. If initialization signal phiINTV and phiSTV are made into a high, presetting of all the circuit stages of the vertical-scanning circuit VSR is carried out, all line Rhine GV1, GV2, and GV3 becomes a high, and all pixels will be in a selection condition. On the other hand, if initialization signal phiINTV is made into a high and scan start signal phiSTV is made into a low, each circuit stage of the vertical-scanning circuit VSR is reset, and all pixels will be in the condition of not choosing. If initialization signal phiINTV is made into a low, the vertical-scanning circuit VSR will start the usual shift action, whenever clock

signal phiCKV enters from the time of start signal phiSTV becoming a high, each line Rhine GV1, GV2, and GV3 serves as a high level one by one, and sequential selection of the pixel of every one line is made.

[0012] And in order to reset all pixels in the solid state camera of drawing 6 , perpendicular read-only reset-signal phiRSTV is first made into a high, the transistors 1-QRSTV 3 for perpendicular reset of each train are set to ON, and each train Rhine LV1, LV2, and LV3 is connected to a gland.

[0013] Next, both said initialization signal phiINTV of the vertical-scanning circuit VSR and scan start signal phiSTV are made into a high, and each circuit stage of the vertical-scanning circuit VSR is changed into a presetting condition. By this, each line Rhine GV1, GV2, and GV3 of both becomes high-level, and will be in the selection condition of all pixels. The high-level electrical potential difference of each line Rhine GV1, GV2, and GV3 in this case, i.e., the electrical potential difference of control signal phiSRs 1-3, is set up so that it may become the electrical potential difference VRSTP for reset of static inductions transistor 11-QS 33.

[0014] As everyone knows, an inversion layer is formed in the gate electrode lower part of each static inductions transistor QS11-QS33, a channel is made

between the source drains of these static inductions transistor 11-QS 33, the residual charge charged at the gate flows out, and reset of all pixels is performed by this. At this time, the current by the outflow of the residual charge by reset flows at coincidence to the static inductions transistor QS11-QS33 of each pixel.

[0015]

[Problem(s) to be Solved by the Invention] Thus, in the solid state camera which has the conventional magnification mold image sensor, when all pixels were reset, it was resetting by making a picture element part including a magnification means into one by choosing all pixels as coincidence. For this reason, at the time of reset, all the magnification means in each pixel are also turned on at coincidence, and the currents of all magnification means flow all at once. Although the current at this time is called rushes current, since all pixels become small [the rushes current of each pixel] with ON at coincidence, a big rushes current flows with the whole image pick-up equipment.

[0016] For example, though the rushes current of each pixel is several microampere, when the number of pixels is 1 million pixels, with the whole image pick-up equipment, it amounts to several A. When the current which reaches in the chip of a solid state camera at several A flowed, there was also a possibility

of the fall of the dependability by electromigration becoming a problem, and the electrical potential difference of each [in a chip] part having not fitted in the predetermined electrical-potential-difference range with the parasitism impedance of each part in a chip, and the engine performance which the chip expected as a solid state camera not having been demonstrated, or producing malfunction by the rushes current etc.

[0017] Therefore, the purpose of this invention is to enable it to also prevent the fall of the dependability of a solid state camera exactly while the excessive rushes current at the time of reset is prevented in the solid state camera which used the pixel of a magnification mold and the whole chip of a solid state camera enables it to demonstrate the predetermined engine performance in view of the trouble in such conventional equipment.

[0018]

[Means for Solving the Problem] In the solid state camera possessing the scanning circuit for according to the 1st **** of this invention, making sequential selection and reading two or more pixels which perform photo electric conversion, and said two or more pixels, in order to attain the above-mentioned purpose Tandem connection of two or more circuit stages should be carried out,

and said scanning circuit should be constituted, and should equip coincidence with the shift register which can be set as a predetermined logic state for the output of two or more of said circuit stages mostly according to the input of a predetermined control signal. The photo detector in which said pixel accumulates the signal charge according to a lightwave signal at least respectively, While choosing two or more pixels by having had the amplifier which amplifies the signal charge accumulated in this photo detector, and setting the output of two or more circuit stages of the shift register of said scanning circuit as said predetermined logic state The rushes current at the time of reset is reduced by resetting the charge of said photo detector, where said amplifier is cut off in two or more selected pixels.

[0019] With such a configuration, where said amplifier is cut off in two or more pixels which chose and chose two or more pixels with the shift register of said scanning circuit, the charge of said photo detector is reset. Therefore, it is lost that a rushes current flows to an amplifier at the time of reset, and even if it resets to coincidence all the pixels in the solid state camera which has many pixels, it is lost that an excessive rushes current flows. Therefore, it becomes without the dependability of a solid state camera not falling and moreover the

electrical potential difference of each part in the chip of a solid state camera causing big fluctuation by the rushes current, and a solid state camera can demonstrate the original engine performance now exactly.

[0020] In this case, the transfer component which transmits the signal charge by which said pixel was further accumulated in said photo detector in each to the control electrode of said amplifier, and the reset component which resets the charge of the control electrode of said amplifier shall be provided, and the charge of a photo detector shall be reset by setting both said transfer component and said reset component to ON.

[0021] By taking such a pixel configuration, it becomes possible to emit the charge accumulated in the photo detector through said transfer component and a reset component, where an amplifier is cut off by applying the electrical potential difference which sets said transfer component and reset component to ON at both the times of reset, and cuts off this amplifier to the control electrode of an amplifier through a reset component.

[0022] Furthermore, in case the charge of a photo detector is reset by setting both said transfer component and a reset component to ON, it can also constitute so that the bias voltage impression means for impressing bias voltage

to said amplifier and holding said amplifier in the cut-off condition may be included.

[0023] In this case, the bias voltage for changing said amplifier into a cut-off condition to said amplifier at the time of reset of a pixel with the above-mentioned bias voltage impression means can be impressed. Therefore, the property of a photo detector and an amplifier can be set as the independently optimal respectively thing, where an amplifier is cut off completely, perfect depletion-ization of a photo detector can be attained, the degree of freedom of a design of each component increases, and the solid state camera of high quality can be realized.

[0024] Moreover, two or more pixels which consist of a magnification mold photo-electric-conversion means to be arranged in the shape of two-dimensional in a line and the direction of a train, and to accumulate and amplify the signal charge according to a lightwave signal respectively in other **** of this invention, In the current regulator circuit prepared for each [which connected in common the output terminal of each pixel arranged in the direction of a train] train Rhine of every, and the solid state camera which carries out the selection drive of said pixel and which has level and perpendicular each scanning circuit Tandem

connection of two or more circuit stages should be carried out, and said vertical-scanning circuit should be constituted, and should equip coincidence with the shift register which can be set as a predetermined logic state for the output of two or more of said circuit stages mostly according to the input of a predetermined control signal. Said pixel respectively the signal charge according to a lightwave signal The photo detector to accumulate, the amplifier which amplifies the signal charge accumulated in this photo detector, the transfer component which transmits the signal charge accumulated in said photo detector to the control electrode of said amplifier, and the reset component which resets the charge of the control electrode of said amplifier are provided. The control electrode of the transfer component of the pixel of each line is connected to line Rhine which corresponds in common, line Rhine of each line is connected to the correspondence circuit stage of said vertical-scanning circuit, and the control electrode of the reset component of all pixels is connected to a reset control signal input terminal in common. And all transfer components are set to ON through said each line Rhine by setting the output of two or more circuit stages of the shift register of said vertical-scanning circuit as said predetermined logic state. And while setting the reset component of all pixels to

ON and resetting the charge of a photo detector through a transfer component and a reset component by adding said reset control signal to the reset component of all pixels By impressing the electrical potential difference which makes this amplifier a cut-off condition to the control electrode of an amplifier through the reset component which became ON on the occasion of this reset, the rushes current at the time of reset is reduced.

[0025] It can set to the solid state camera concerning such a configuration, and all the transfer components of each line Rhine can be set to ON by making the output of two or more circuit stages of the shift register of said vertical-scanning circuit into a predetermined logic state at the time of reset, and the reset component of all pixels can be set to ON, and the charge of a photo detector can be reset through a transfer component and a reset component. Moreover, if the electrical potential difference which makes this amplifier a cut-off condition is impressed to the control electrode of an amplifier through the reset component which became ON on the occasion of this reset, it is lost that a rushes current flows to an amplifier at the time of reset, and even if it resets many pixels to coincidence, it will be lost that a rushes current excessive as the whole solid state camera flows.

[0026] In **** of further others of this invention The current regulator circuit prepared for each [which connected in common the output terminal of two or more pixels which consist of a magnification mold photo-electric-conversion means to be arranged in the shape of two-dimensional in a line and the direction of a train, and to accumulate and amplify the signal charge according to a lightwave signal respectively, and each pixel arranged in the direction of a train] train Rhine of every, and said pixel In the solid state camera which has horizontal and perpendicular each scanning circuit which carries out a selection drive Tandem connection of two or more circuit stages should be carried out, and said vertical-scanning circuit should be constituted, and should equip coincidence with the shift register which can be set as a predetermined logic state for the output of two or more of said circuit stages mostly according to the input of a predetermined control signal. Said pixel respectively the signal charge according to a lightwave signal The photo detector to accumulate, the amplifier which amplifies the signal charge accumulated in this photo detector, the transfer component which transmits the signal charge accumulated in said photo detector to the control electrode of said amplifier, and the reset component which resets the charge of the control electrode of said amplifier are provided.

The control electrode of the transfer component of the pixel of each line is connected to line Rhine which corresponds in common, line Rhine of each line is connected to the correspondence circuit stage of said vertical-scanning circuit, and the control electrode of the reset component of all pixels is connected to a reset control signal input terminal in common. Moreover, it has a means to impress bias voltage to an amplifier through each train Rhine in order that each train Rhine may change into a cut-off condition the amplifier of the pixel connected to each train Rhine. And all transfer components are set to ON through said each line Rhine by setting the output of two or more circuit stages of the shift register of said vertical-scanning circuit as said predetermined logic state. And while setting the reset component of all pixels to ON and resetting the charge of a photo detector through a transfer component and a reset component by adding said reset control signal to the reset component of all pixels By making the amplifier of all pixels into a cut-off condition with said bias voltage impression means in the case of this reset, the rushes current at the time of reset is reduced.

[0027] The charge of a photo detector can be emitted through a transfer component and a reset component by setting all transfer components to ON through each line Rhine, and setting the reset component of all pixels to ON with

said reset control signal by setting the output of two or more circuit stages of the shift register of a vertical-scanning circuit as a predetermined logic state also in this case. And the rushes current at the time of reset can be reduced by making the amplifier of all pixels into a cut-off condition with said bias voltage impression means in the case of this reset. Since said bias voltage impression means can impress desired suitable bias voltage to the amplifier of a pixel independently with other components, it can increase the degree of freedom of a design of each component of a pixel. That is, through said transfer component and a reset component, the electrical potential difference by which a photo detector is depletion-ized completely can be supplied, and the bias voltage which fully makes this amplifier a cut-off condition on the other hand at said amplifier can be impressed independently, and it can design so that it may have the optimal property of respectively a request of a photo detector and an amplifier.

[0028]

[Embodiment of the Invention] Drawing 1 is the block diagram showing the configuration of the outline of the solid state camera concerning this invention, and shows the example of two-dimensional image sensors. The solid state camera of this drawing is equipped with the picture element part 3 which has two

or more pixels 1, the vertical-scanning circuit 5, the level read-out section 7, and the horizontal scanning circuit 9.

[0029] The pixel 1 equipped with a photodiode, an amplifier, etc. for light-receiving so that it might explain to a detail later, respectively is arranged in the shape of a matrix, and the picture element part 3 is constituted. The vertical-scanning circuit 5 makes sequential selection of the pixel for 1 level Rhine (line Rhine) of a picture element part 3, and consists of dynamic shift registers of the structure shown later. The level read-out section 7 receives the charge of the pixel for 1 level Rhine from a picture element part 3, and carries out the sequential output of this based on the scan pulse from the horizontal scanning circuit 9. The horizontal scanning circuit 9 is also constituted by the same dynamic shift register as said perpendicular criminal-investigation circuit 5.

[0030] Signal phiSTV inputted into the vertical-scanning circuit 5 is a perpendicular start pulse, and serves as a dynamic shift register's initial input data. Moreover, perpendicular clock pulse phiCKV for shifting the dynamic shift register and perpendicular initialization pulse phiINTV are inputted into the vertical-scanning circuit 5.

[0031] Moreover, signal phiSTH inputted into the horizontal scanning circuit 9 is

the start signal of the dynamic shift register who constitutes the horizontal scanning circuit 9, and phiCKH is a clock signal for a level shift. Moreover, level initialization pulse phiINTH for initializing the dynamic shift register who constitutes this horizontal scanning circuit 9 if needed is inputted into the horizontal scanning circuit 9.

[0032] In the solid state camera of drawing 1 , when used, for example for a still video camera etc., before pushing a shutter, a solid state camera carries out false actuation, namely, although a scan is carried out, the output signal is made into the condition of not using it. And if a shutter is pushed, fixed period initialization pulse phiINTV for about 10 microseconds will be added to the vertical-scanning circuit 5 and start pulse phiSTV will be made into H level at coincidence, the whole page of the shift register of the vertical-scanning circuit 5 under false actuation will be in a presetting condition compulsorily, all pixels will be in a selection condition, and the charge of all pixels can be reset.

[0033] Next, after make perpendicular start pulse phiSTV into L level, and making the vertical-scanning circuit 5 into a reset condition, adding initialization pulse phiINTH also to the horizontal scanning circuit 9, and making level start pulse phiSTH into L level and changing the horizontal scanning circuit 9 into a

reset condition, it returns to normal operation and the shift action of each shift register is started. At this time, each pixel has started are recording of image information, and if it returns to the usual actuation and read-out actuation is started after it makes L level again H level, and perpendicular start pulse phiSTV and level start pulse phiSTH for initialization pulse phiINTV and phiINTH after progress of the predetermined exposure time and carries out forcible reset of each shift register, it can acquire the predetermined video signal by which time amount exposure was carried out.

[0034] In addition, in the solid state camera of drawing 1 , the usual read-out actuation is in the condition which made the low each initialization pulse phiINTV of the vertical-scanning circuit 5 and the horizontal scanning circuit 9, and phiINTH, respectively, carries out the sequential shift of the start signal phiSTV of a high level by clock signal phiCKV in the vertical-scanning circuit 5, and makes sequential selection of the pixel for 1 level Rhine of a picture element part 3. The charge accumulated in the photodiode of each pixel for selected 1 level Rhine is transmitted to the level read-out section 7. Next, by carrying out the sequential shift of start signal phiSTH of a high level clock signal phiCKH by the horizontal scanning circuit 9, by this horizontal scanning circuit 9, the charge

transmitted to the level read-out section 7 is horizontally transmitted one by one by 1 pixel, and it reads outside from an output terminal.

[0035] Drawing 2 shows the detailed circuitry of the solid state camera of drawing 1 . The same part as drawing 1 is shown by the same reference figure in the solid state camera of drawing 2 . That is, it is constituted by the picture element part 3 which the solid state camera of drawing 2 also equipped with two or more pixels 1, the vertical-scanning circuit 5, the level read-out section 7, the horizontal scanning circuit 9, etc. In the circuit of drawing 2 , the picture element part 3 shall consist of pixels 1 of three line x3 train for simplification of explanation.

[0036] Each pixel 1 consists of reset switches QRST which consist of an MOS transistor for setting the switch QT for a transfer which consists of an MOS transistor for transmitting the charge of Amplifier QA and Photodiode PD which consist of a photodiode PD which is a photo detector, and a junction field effect transistor (JFET) to the gate of Amplifier QA, and the gate electrode of Amplifier QA as a predetermined electrical potential difference. In addition, in a drawing, although the subscript is made each component, when expressing on behalf of the component of the same class for simplification of explanation, a subscript

may be omitted. In each pixel 1 shown in drawing 2 , the gate of the photodiode PD which is a light-receiving means, and Amplifier QA is separated on structure.

[0037] The source of the amplifier QA of the pixel perpendicularly arranged among the amplifiers QA of each pixel 1 is connected to the constant current source CSV of each train through train Rhine LV of each train (LV1-LV3). Each constant current source CSV serves as a load when operating Amplifier QA as a source follower. The other end of each constant current source CSV is connected to the predetermined power source VEE in common.

[0038] The cathode of the photodiode PD of each pixel 1 is connected to the predetermined power source VDD in common, and the anode is connected to the source of the switch QT for a transfer. The drain of the switch QT for a transfer is connected to the gate of Amplifier QA, and the source of a reset switch QRST. The source of each amplifier QA is connected to each train Rhine LV (LV1-LV3) in common for every train. The gate of each switch QT for a transfer is constituted so that it may connect with the vertical-scanning circuit 5 in common for every line and 1st vertical-scanning signal phiTR may be received. Vertical-scanning signal phiTR1 of each line - phiTR3 are connected to the output of each circuit stage of the vertical-scanning circuit 5. The gate of a reset

switch QRST is connected to control signal phiPG [all / pixel], and the drain is constituted so that it may connect with the vertical-scanning circuit 5 in common horizontally and 2nd vertical-scanning signal phiRD may be supplied for every line. The drain of each amplifier QA is connected to the power source VDD same in common as the anode of said photodiode PD.

[0039] In addition, since the output of each circuit stage of the vertical-scanning circuit 5 supplies the 1st [of a voltage level], and 2nd vertical-scanning signal phiTR(s) different, respectively and phiRD, it can also connect and constitute a predetermined electrical-potential-difference shift circuit in the output of each circuit stage of a shift register, respectively.

[0040] The level read-out section 7 is read for every train, and consists of a gate transistor QTC, capacity CT, and a switching device QH for level read-out. The upper limit of each train Rhine LV is connected to the drain of the read-out gate transistor QTC, and the source of this read-out gate transistor QTC is connected to the drain of the switching device QH for level read-out of each train, and capacity CT. The other end of capacity CT is grounded. The gate of all the read-out gate transistors QTC is constituted so that it may connect in common and transfer pulse phiT can be supplied. Moreover, the gate of the switching

device QH for level read-out is connected to the output of each circuit stage of the shift register of the horizontal scanning circuit 9 for every train. Furthermore, the source of the switching device QH for level read-out is connected to the video outlet terminal through the water Hiraide line of force HOUT in common.

[0041] In the solid state camera which has the above configurations, reset of a pixel is performed as follows. That is, both initialization pulse phiINTV of the vertical-scanning circuit 5 and start pulse phiSTV are made into a high, and all the circuit stages of the vertical-scanning circuit 5 are preset, and it considers as the selection condition of all pixels. By this, all (phiTR1 - phiTR3) of 1st vertical-scanning signal phiTR of all circuit stages are made into a high at coincidence, and the switch QT for a transfer of all pixels is set to ON. Moreover, reset control signal phiPG common to all pixels is added, and the reset switch QRST of all pixels is turned ON.

[0042] Let the electrical potential difference of 2nd vertical-scanning signal phiRD (phiRD1 - phiRD3) be the electrical potential difference VGL which JFET which constitutes the amplifier QA of each pixel cuts off at this time.

[0043] thus, when it carries out, the residual charge accumulated in the photodiode PD of each pixel is discharged through the transfer component QT

and the reset component QRST, and Photodiode PD is perfect -- depletion -- it is-izing and reset. And since the gate voltage of Amplifier QA is VGL as mentioned above, therefore this amplifier QA has cut off in this case, a current does not flow to this amplifier QA. That is, the current with which the current which flows to Photodiode PD was amplified and amplified by Amplifier QA does not flow. For this reason, the rushes current of each pixel becomes very small, and it is lost that a rushes current excessive as the whole solid state camera flows.

[0044] In addition, while making initialization pulse phiINTV of the vertical-scanning circuit 5 into a low level and making start pulse phiSTV into a high, clock signal phiCKV is added and the shift action of the vertical-scanning circuit 5 is made to perform, when reading a signal in the solid state camera of drawing 2 . By this, sequential selection of the pixel of each line is made, and the signal accumulated in the selected pixel is outputted to the perpendicular read-out line LV. And it connected with each train Rhine, and reads, the gate transistor QTC is set to ON by transfer pulse phiT, and the read-out charge of a signal is charged at the capacity CT of each train. Moreover, a shift action is made to perform also in the horizontal scanning circuit 9 by making a low level

and start pulse phiSTH high-level for initialization pulse phiINTH, and adding clock signal phiCKH. The switching device QH for level read-out of each train is considered as sequential ON, and the read-out signal of each train is supplied to water Hiraide force Rhine HOUT by this, and is outputted outside from a video outlet terminal.

[0045] Moreover, in reading such a signal, it turns ON the reset component QRST of all pixels by reset control signal phiPG. And to the selected line, make the electrical potential difference of 2nd vertical-scanning signal phiRD into the electrical potential difference VGH which the amplifier QA of each pixel is turned on and activates, and let it be said electrical potential difference VGL which Amplifier QA cuts off to a non-choosing pixel. In this condition, in said control signal phiPG, even if off, the gate voltage of this amplifier QA is held with the gate stray capacity of Amplifier QA at the same value. Therefore, after turning OFF the reset component QRST of all pixels by reset control signal phiPG, the transfer component of the pixel of the line chosen by 1st vertical-scanning signal phiTR is turned ON. The signal charge accumulated in Photodiode PD is transmitted to the gate of Amplifier QA by this, and the gate voltage of this amplifier QA changes with it corresponding to a signal. Amplifier QA is operated

as a source follower, this electrical potential difference is outputted to train Rhine LV, the horizontal scanning circuit 9 is scanned as mentioned above, and it reads outside one by one.

[0046] Drawing 3 shows an usable dynamic shift register's configuration to the horizontal scanning circuit and vertical-scanning circuit of a solid state camera concerning this invention. The dynamic shift register of drawing 3 is created using a CMOS process, and shows the example which used the so-called clocked inverter in which sequential activation is carried out by the clock pulse.

[0047] In the dynamic shift register of drawing 3 , two PMOS transistors P1 and P2 and two NMOS transistors N2 and N1 by which the series connection was carried out, for example between the forward supply voltage VDD and the negative supply voltage VSS constitute one step of clocked inverter. The PMOS transistors P3 and P4 and the NMOS transistors N4 and N3 constitute the 2nd step of clocked inverter, the PMOS transistors P5 and P6 and two NMOS transistors N6 and N5 constitute the 3rd step of clocked inverter, two PMOS transistors P7 and P8 and two NMOS transistors N8 and N7 constitute the 4th step of clocked inverter, and it is the same as that of the following.

[0048] P2 and the 2 or 2nd step of N constitute P8, N8, and a ********** CMOS

inverter from P6 and the 6 or 4th step of N by P4 and the 4 or 3rd step of N at the PMOS transistor located in the center in the clocked inverter of each circuit stage, and the NMOS transistor, for example, the 1st step. The transistor connected between each CMOS inverter and power sources VDD and VSS is a transistor for control for activating these CMOS inverters.

[0049] The PMOS transistors P1 and P5 and the gate of -- are connected to the internal clock signal line CP 1 among these transistors for control, and the PMOS transistors P3 and P7 and the gate of -- are connected to the internal clock signal line CP 2. Moreover, the transistor N1 and N5 for control of other electric conduction forms, i.e., NMOS transistors, and the gate of -- are connected to the internal clock signal line CN1, and the gate is connected to other internal clock signal lines CN2 of the NMOS transistors N3 and N7 and --.

[0050] Moreover, start pulse phiST is supplied to the gate of each transistors P2 and N2 which constitute the 1st step of CMOS inverter. The 1st step of output of a CMOS inverter is connected to the gate of the 2nd step of input P4 of a CMOS inverter, i.e., a transistor, and a transistor N4, the 2nd step of output of a CMOS inverter is connected to the 3rd step of output of a CMOS inverter, and sequential connection of the 3rd step of output of a CMOS inverter is made at

the 4th step of input of a CMOS inverter.

[0051] The dynamic shift register of drawing 3 had further the inverter INV2 and the OR gates OR1 and OR2 which constitute a coincidence activation circuit, and has two more inverters INV3 and INV4. Initialization pulse phiINT is supplied to one [each] input of the OR gates OR1 and OR2. As for the input of another side of OR-gate OR1, clock pulse phiCK is supplied, and the signal to which the input of another side of other OR-gate OR2 reversed clock pulse phiCK with the inverter INV2 is supplied. It connects with said internal clock signal line CN2, and the output of OR-gate OR1 is connected to the internal clock signal line CP 2 through the inverter INV4. It connects with the internal clock signal line CN1, and the output of OR-gate OR2 is connected to the internal clock signal line CP 1 through the inverter INV3.

[0052] In the dynamic shift register who has the above configurations, when initialization pulse phiINT is low (L) level, clock pulse phiCK occurs in the output of OR-gate OR1, and the clock pulse which reversed clock pulse phiCK is supplied to the output of OR-gate OR2. Therefore, when clock pulse phiCK is high (H) level, H level and the internal clock signal line CP 2 serve as [the internal clock signal line CN2] L level, and transistors P3 and P7, -- and N3 and

N7, and -- become ON. On the other hand, when clock signal phiCK is L level, the output of OR-gate OR2 serves as H level, and transistors P1 and P5, -- and N1 and N5, and -- become ON. Therefore, the 1st inverter and 2nd inverter of each circuit stage are activated by turns by clock signal phiCK, and start pulse phiST is shifted to the circuit stage of sequential consecutiveness.

[0053] on the other hand -- if initialization pulse phiINT is made into H level -- the level of clock pulse phiCK -- both the outputs of the OR gates OR1 and OR2 serve as H level irrespective of how. Therefore, both the internal clock signal lines CN1 and CN2 serve as H level, and both the internal clock signal lines CP1 and CP2 serve as L level. For this reason, the transistors P1, P3, P5, and P7 for control of all clocked inverters, -- and N1, N3, N5 and N7, and -- become coincidence with ON. That is, all clocked inverters are activated by coincidence.

[0054] Regardless of clock pulse phiCK, it is reversed with each inverter, and input signal phiST is high-speed and is transmitted to a latter circuit by this. Therefore, if start pulse phiST is made into L level, all also of the outputs S1 and S2 of all circuit stages and -- will be set to L level, and the outputs S1 and S2 of H level, then all circuit stages and -- will be set to H level in start pulse phiST. That is, the output to all circuit stages or a desired circuit stage can be set or

preset almost in instant. Moreover, since all circuits are in an active state, it is stabilized and they can also carry out long duration continuation of reset or the presetting condition. In addition, the time delay of the clocked inverter used for the usual solid state camera is usually several or less nanoseconds, even if it has 1000 steps of clocked inverters, transfer of data will be possible for it in several or less microseconds from an input stage to the last stage, and it can perform reset or presetting of each circuit stage mostly in an instant.

[0055] Drawing 4 shows other examples of a configuration of a dynamic shift register which can be used for the solid state camera of this invention. The dynamic shift register of drawing 4 has two CMOS inverters for every circuit stage. That is, the 1st circuit stage has the 1st CMOS inverter which consists of a PMOS transistor P11 and an NMOS transistor N11, and the 2nd CMOS inverter which consists of a PMOS transistor P12 and an NMOS transistor N12. The 2nd circuit stage is equipped with the 1st CMOS inverter which consists of a PMOS transistor P13 and an NMOS transistor N13, and the 2nd CMOS inverter which consists of a PMOS transistor P14 and an NMOS transistor N14, and is the same as that of the following. Cascade connection of each inverter is carried out one by one through the transmission gate. Namely, the output of the inverter

which consists of transistors P11 and N11 is connected to the input of the inverter which consists of transistors P12 and N12 through the 1st transmission gate T1. The output of the inverter which consists of transistors P12 and N12 is connected to the input of the inverter which consists of transistors P13 and N13 through the 2nd transmission gate T2. It connects with the input of the inverter which consists of transistors P14 and N14 through 3rd transmission gate T3, and the output of the inverter which consists of transistors P13 and N13 is the same as that of the following.

[0056] The gate by the side of a transmission gate T1, T3, and the PMOS transistor of -- is connected to the internal clock signal line CP 1, and the gate of an NMOS transistor is connected to the internal clock signal line CN1. Moreover, the gate of a transmission gate T2, T four, and the PMOS transistor of -- is connected to the internal clock line CP 2, and the gate of an NMOS transistor is connected to the internal clock signal line CN2.

[0057] The dynamic shift register of drawing 4 has the inverter INV2 and the coincidence activation circuit which consists of the OR gates OR1 and OR2 like the thing of drawing 3 , and has the inverters INV4 and INV3 which reverse the output of the OR gates OR1 and OR2, respectively, and are supplied to the

internal clock signal lines CP2 and CP1. The output of the OR gates OR1 and OR2 is connected to the internal clock signal lines CN2 and CN1 again.

[0058] In the dynamic shift register of drawing 4 , when initialization pulse phiINT is L level, the reversal clock pulse to which the output of the OR gates OR1 and OR2 reversed clock pulse phiCK and this clock pulse phiCK, respectively is outputted. These clock pulse phiCK and the reversal clock pulse of those are supplied to the internal clock signal lines CN2 and CN1, respectively. Moreover, it is further reversed with inverters INV4 and INV3, respectively, and clock pulse phiCK outputted from the OR gates OR1 and OR2, respectively and its reversal clock pulse are supplied to the internal clock signal lines CP2 and CP1, respectively. That is, clock pulse phiCK is supplied for the clock pulse which reversed clock signal phiCK to the internal clock signal line CP 2 to the internal clock signal line CP 1.

[0059] Therefore, when clock pulse phiCK is H level, a transmission gate T2, T four, and -- flow, and when clock pulse phiCK is L level, a transmission gate T1, T3, and -- flow. That is, a flow and un-flowing transmission gates T1 and T2, T3, T four, and -- are presupposed by turns by clock signal phiCK. It is transmitted to the circuit stage of sequential consecutiveness [like / common knowledge] of

start pulse phiST by this, and a shift action is performed.

[0060] On the other hand, when initialization pulse phiINT is H level, both the outputs of the OR gates OR1 and OR2 serve as H level irrespective of the level of clock pulse phiCK. For this reason, both the H level and internal clock signal lines CP1 and CP2 of both serve as L level, and, as for the internal clock signal lines CN1 and CN2, all the transmission gates T1 and T2, T3, T four, and -- flow. That is, direct cascade connection of the inverter of all circuit stages will be carried out. Therefore, while sequential reversal of the start pulse phiST is carried out, it is directly transmitted by each inverter. Therefore, it becomes possible to also set in the circuit of drawing 4 , and to reset or preset each circuit stage in an instant.

[0061] In addition, in above-mentioned explanation, although explained per two kinds of things as a dynamic shift register, it is clear to this invention that the dynamic shift register of various formats can be used. That is, each circuit stage consists of 1 set of two-step dynamic form inverter circuits, and at the time of an active state, if another side is a dynamic shift register of a format who transmits to the circuit stage of the sequential consecutiveness to an input signal as an inactive condition substantially, this invention is substantially [one of the two]

applicable. 1 set of two-step dynamic form inverters can be activated to coincidence in these cases, an input signal can be transmitted to the circuit stage of direct consecutiveness over two or more circuits stage, and reset and presetting can be made to perform compulsorily in an instant.

[0062] Next, drawing 5 shows the circuitry of the solid state camera concerning another ******** of this invention. Also in drawing 5 , the same part as said drawing 1 is shown by the same reference figure. Moreover, in the solid state camera of drawing 5 , each train Rhine LV1, LV2, and LV3 in the solid state camera of said drawing 2 is connected to the predetermined bias voltage VPU through the switching devices QPU1, QPU2, and QPU3 which consist of MOS transistors for pull-up etc., respectively. The gate of each switching devices QPU1, QPU2, and QPU3 is constituted so that it may connect in common and predetermined control signal phiPU can be supplied. Moreover, even if the gate of Amplifier QA is the read-out electrical potential difference VGH of Amplifier QA, let bias voltage VPU be the electrical potential difference which this amplifier QA cuts off. Other parts are the same as the circuit of drawing 2 , and the same reference figure and the same reference mark are given to the same part.

[0063] In resetting a pixel in the solid state camera of drawing 5 , like the case of

drawing 2 , the whole page of the vertical-scanning circuit 5 is preset, the 1st vertical-scanning circuit phiTR1-TR3 is added to the switch QT for a transfer of all pixels, and it sets this switch QT for a transfer to ON. Moreover, control signal phiPG is added and the reset switch QRST of all pixels is turned ON. Let the electrical potential difference of 2nd vertical-scanning signal phiRD1 - phiRD3 be the read-out electrical potential difference VGH of the amplifier QA of each picture element part at this time.

[0064] Furthermore, bias of each train Rhine LV1-LV3 is carried out to said bias voltage VPU by control signal phiPU by setting the switching device QPU for pull-up of each train to ON at this time. As mentioned above, the gate of Amplifier QA reads this bias voltage VPU, and even if it is an electrical potential difference VGH, let it be the electrical potential difference which Amplifier QA cuts off. By this, where Amplifier QA is cut off, the residual charge of Photodiode PD is emitted through the transfer component QT and the reset component QRST, and reset of a pixel is performed. And Photodiode PD is reset in this case by the condition that the reverse bias was carried out to the read-out electrical potential difference VGH of Amplifier QA. However, by the switching device QPU for pull-up, the source electrical potential difference of each amplifier QA is said

bias voltage VPU, and a current does not flow to Amplifier QA. That is, the excessive rushes current at the time of reset can be prevented. In addition, when reading a signal, where the switching device QPU for pull-up is considered as a cut-off, it carries out like the case of the solid state camera of said drawing 2 .

[0065] In the solid state camera of above-mentioned drawing 2 and drawing 5 , it is desirable to constitute as a property of the photo detector of each pixel, so that perfect depletion may be formed at the time of reset. However, if the property of JFET which constitutes Amplifier QA if manufacture process conditions are set up so that such a photo detector may be constituted may not be enough and thinks the property of JFET as important conversely, perfect depletion-ization of a photo detector may be unable to be attained. Therefore, when both the JFET properties of the photodiode of a photo detector and an amplifier are compatible with a desired property, when coexistence is difficult or impossible, considering as the configuration of drawing 5 is desirable [considering as the configuration of said drawing 2 is desirable, and].

[0066]

[Example] In addition, in the solid state camera in above-mentioned drawing 2 and drawing 5 , the electrical potential difference of each power source and a

signal is specifically set up as follows, and a high result is obtained. That is, it is referred to as read-out electrical-potential-difference VGH=-1V which the amplifier QA of each of said pixel is turned on, and activates on condition that supply voltage VDD=5V and VEE=0V. And the electrical potential difference VGL of 2nd vertical-scanning signal phiRD supplied to the drain of the reset component of each pixel at the time of the reset in the configuration of said drawing 2 is good -3V. Moreover, bias voltage VPU for cutting off each pixel in the configuration of said drawing 5 is made into the electrical potential difference (more than +1V [for example,]) which this amplifier QA cuts off even if the gate voltage of Amplifier QA is VGH=-1V.

[0067]

[Effect of the Invention] As mentioned above, since according to this invention it constituted in the solid state camera so that a photo detector might be reset, where the amplifier of each pixel is cut off when resetting, also when resetting the solid state camera smell all pixel containing many pixels to coincidence, it can prevent that an excessive rushes current occurs. Therefore, while being able to prevent the fall of the dependability of the solid state camera by the rushes current, it enables it for having a bad influence on a solid state camera to

be prevented by the voltage variation of each part of the inside of a chip by the rushes current, and to demonstrate the engine performance of original [solid state camera] by it. At the moment of turning off a shutter, all pixel coincidence reset can use such a solid state camera for a required electronic "still" camera etc., and it can obtain a good result.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the configuration of the outline of the solid state image sensor concerning this invention.

[Drawing 2] It is the electrical diagram showing the detailed configuration of the solid state camera concerning the 1st operation gestalt of this invention.

[Drawing 3] It is the electrical diagram showing the configuration of an usable shift register in the scanning circuit of the solid state camera concerning this invention.

[Drawing 4] It is the electrical diagram showing other configurations of an usable shift register in the scanning circuit of the solid state image sensor concerning this invention.

[Drawing 5] It is the electrical diagram showing the detailed configuration of the solid state image sensor concerning the 2nd operation gestalt of this invention.

[Drawing 6] It is the electrical diagram showing the configuration of the conventional solid state camera.

[Description of Notations]

1 Pixel

3 Picture Element Part

5 Vertical-Scanning Circuit (VSR)

7 Level Read-out Section

9 Horizontal Scanning Circuit (HSR)

PD11, --, PD33 Photodiode

QT11, --, QT33 Transfer component

QA11, --, QA33 Amplifier

QRST11, --, QRST33 Reset component

CSV1, --, CSV3 Constant current source

QTC1, --, QTC3 Read-out gate transistor

CT1, --, CT3 Capacity for are recording

QH1, --, QH3 Switching device for level read-out

QPU1, --, QPU3 Switching device for pull-up